1. (Original) A method of forming a MOS transistor comprising:

forming lightly and heavily doped source/drain regions adjacent to one another in a substrate having a gate electrode with a sidewall spacer thereon;

saliciding a surface of the heavily doped source/drain region to provide a first silicide layer self-aligned to the sidewall spacer;

removing at least a portion of the sidewall spacer to expose a portion of the lightly doped source/drain region adjacent to the first silicide layer; and

saliciding the exposed portion of the lightly doped source/drain region to provide a second silicide layer between the first silicide layer and the gate electrode.

2. (Original) The method according to Claim 1 wherein forming lightly and heavily doped source/drain regions comprises:

forming an I-shaped sidewall spacer on the gate electrode; and

forming an L-shaped sidewall spacer including a first portion on the I-shaped sidewall spacer having a base portion on the substrate and a second portion that extends on the substrate from the base away from the gate electrode.

3. (Original) The method according to Claim 1 wherein forming lightly and heavily doped source/drain regions comprises:

forming an L-shaped sidewall spacer including a first portion on the sidewall of the gate electrode having a base portion on the substrate and a second portion that extends on the substrate from the base away from the gate electrode.

4. (Original) The method according to Claim 2 wherein the step of removing at least a portion of the sidewall spacer comprises removing the L-shaped spacer.

5. (Original) The method according to Claim 1 wherein the first and second silicide layers comprise separate silicide layers.

6. (Original) The method according to Claim 1 wherein the step of forming lightly and heavily doped source/drain regions comprises:

forming the lightly doped source/drain region in the substrate self-aligned to the gate electrode;

forming a first spacer on a sidewall of the gate electrode;

forming a second spacer on the first spacer; and

forming the heavily doped source/drain region in the substrate self-aligned to the second spacer.

7. (Original) The method according to Claim 1 wherein the first and second silicide layers form a continuous silicide layer on the heavily doped source/drain region and on the lightly doped source/drain region

8. (Original) The method according to Claim 1 wherein the second silicide layer has a thickness less than that of the first silicide layer.

9. (Original) A method of forming a MOS transistor comprising:

forming lightly and heavily doped source/drain regions adjacent to one another in a substrate having a gate electrode with a sidewall spacer thereon;

forming a first silicide layer having a first thickness on the heavily doped source/drain region self-aligned to the sidewall spacer; and

forming a second silicide layer having a second thickness, less than the first thickness, on the lightly doped source/drain region adjacent to the first silicide layer.

10. (Original) The method according to Claim 9 wherein a surface of the first silicide layer extends beyond a surface of the second silicide layer.

11. (Original) A method of fabricating a MOS transistor comprising:

forming a field region at a substrate to define an active region;

forming a gate electrode on the active region, wherein a gate insulation layer is intervened between the active region and the gate electrode;

forming a lightly doped region in the active region by using the gate electrode and the field region as an ion implantation mask;

forming a gate spacer on sidewalls of the gate electrode, wherein the gate spacer includes a patterned inner insulation layer and a patterned outer insulation layer;

forming a heavily doped region in the active region by using the gate electrode, the gate spacer, and the field region as an ion implantation mask;

removing the patterned outer insulation layer to form an L-shaped spacer on the sidewalls of the gate electrode, wherein the L-shaped spacer is formed of an I-shaped main portion and a projected portion extended from a bottom of the main portion;

forming a first silicide layer on a surface of the heavily doped region adjacent to the L-shaped spacer;

removing the projected portion of the L-shaped spacer to form an I-shaped spacer and to expose a partial surface of the lightly doped region; and

forming a second silicide layer on the exposed lightly doped region.

12.-35. (Canceled)